THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN A. FIFIELD,
DUANE E. GALBI
and
HSING-SAN LEE

Appeal No. 95-2675
Application 07/785,625[1]

ON BRIEF

Before CARDILLO, BARRETT and FLEMING, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

[1] Application for patent filed October 31, 1991. According to appellants, the application is a continuation-in-part of Application 07/517,896, filed April 16, 1990, now U.S. Patent No. 5,307,356 issued April 26, 1994.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 3, 5 through 7, and 9 through 13, all of the claims pending in the application. Claims 4 and 8 have been allowed.

The invention is directed to an on-chip ECC system for DRAMs. More specifically, the invention is directed to an on-chip ECC system that minimizes access delays imposed by the ECC system. On pages 3 through 7 of the specification, Appellants disclose that the prior art recognizes that ECC circuitry imposes a delay time for DRAMs with on-chip ECC systems. The delay is caused because of the time required to calculate the ECC check bits. On page 9, Appellants disclose that their invention reduces this delay. Appellants disclose a memory array that includes first and second memory array cells where the first memory array cells store the data bits and the second memory array cells store the ECC check bits. The data bits are stored in first memory array cells having a predetermined access speed. While the data bits are being stored, the ECC check bits are calculated and then stored in second memory array cells having a faster access speed than the predetermined access speed of the first array memory cells. Since the second memory array cells

have a faster access speed, the delay of writing to the memory is reduced.

Independent claims 1 and 5 are reproduced as follows:

1. A memory device for reducing or eliminating computer system delay which would otherwise occur in a WRITE operation when part of the data to be written is delayed comprising:

a first plurality of storage cells having a predetermined access time for receiving undelayed data;

at least one additional plurality of storage cells in common array with the first plurality of storage cells and having an access time faster than said predetermined access time for receiving delayed data; and

a single control means for: first addressing and storing undelayed data in selected ones of the first plurality of storage cells, and later addressing and storing delayed data in selected ones of the at least one additional plurality of storage cells.

5. A fast writeback memory device having on-chip ECC circuitry for generating check bits associated with data bits in a data word comprising:

an array of memory cells including a plurality of data bit cells having a predetermined access speed for storing data bits and at least one plurality of check bit cells having relatively faster access time for storing check bits; and

a single control means for first addressing and storing data bits in selected ones of the data bit cells and later addressing and storing check bits in selected ones of the check bit cells.

The Examiner relies on the following references.

Scharrer	4,833,648	May 23, 1989

Kurogawa[2] (Japanese Kokai)	57-143800	Sept. 6, 1982
Sato[3]	1-208,788	Aug. 22, 1989

Claims 1, 5, 10 and 11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kurogawa. Claims 2, 3, 6, 7, 9, 12 and 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kurogawa and Scharrer. Claims 1, 5, 10 and 11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato. Claims 2, 3, 6, 7, 9, 12 and 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato and Scharrer.[4]

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[2] A copy of the translation provided by the U.S. Patent and Trademark Office, September 1993, is included and relied upon for this decision.

[3] A copy of the translation provided by the U.S. Patent and Trademark Office, September 1993, is included and relied upon for this decision.

[4] In the final office action, claims 10 and 11 were rejected under 35 U.S.C. § 112. On page 5 of the answer, the Examiner set forth the title of the paragraph as follows: "REJECTION UNDER 35 U.S.C. 112, second paragraph (claims 10 & 11)." However, the paragraph states that the "final rejection of claims 1-8 under 35 U.S.C. 112, second paragraph, has been withdrawn in view of the remarks set forth on page 8 of appellant's [sic, appellants'] brief." We note on page 2 of the final rejection, the Examiner rejects only claims 10 and 11 under 35 U.S.C. § 112, second paragraph. Although the Examiner has referred to claims 1-8, it is apparent that this was a typographical error and that the Examiner is in fact withdrawing the rejection of claims 10 and 11 under 35 U.S.C. § 112, second paragraph. This is further supported by the fact that the Examiner did not respond to

(continued...)

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[5] and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 1 through 3, 5 through 7, and 9 through 11 are directed to subject matter that would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103. However, we do not agree with the Examiner that claims 12 and 13 are directed to subject matter that would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103.

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[4](...continued)
Appellants' arguments in regard to the rejection of claims 10 and 11 under 35 U.S.C. § 112, second paragraph, and that page number 8 of Appellants' brief referenced by the Examiner pertains to claims 10 and 11 and not to claims 1-8. Therefore, we find that the rejection of claims 10 and 11 under 35 U.S.C. § 112, second paragraph, is withdrawn and is not properly before us for decision.

[5] Appellants filed an appeal brief on July 7, 1994. We will reference this appeal brief as simply the brief. Appellants filed a reply appeal brief on December 7, 1994. We will reference this reply appeal brief as the reply brief. The Examiner stated in the Examiner's letter dated December 19, 1994 that the reply brief was entered into the record.

At the outset, we note that Appellants state on pages 4 and 5 of the brief that claim 11 stands or falls with claim 10 for the rejection of claims 1, 5, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Kurogawa. We also note that on pages 9 through 11 of the brief, Appellants argue claim 1 separately, but fail to present reasons as to why Appellants consider rejected claims 5 and 10 to be separately patentable from claim 1. As per 37 CFR § 1.192(c)(5) as amended at 58 FR 54510 Oct. 22, 1993, which was controlling at the time of Appellants filing the brief, "it will be presumed that the rejected claims stand or fall together unless a statement is included that the rejected claims do not stand or fall together, and in the appropriate part or parts of the argument under subparagraph (c)(6) of this section appellant presents reasons as to why appellant considers the rejected claims to be separately patentable." Appellants have not met the requirements of this rule for claims 1, 5 and 10 to be treated separately. We will, thereby, consider Appellants' claims 1, 5, 10 and 11 as standing or falling together as one group and will treat claim 1 as a representative claim of that group for the rejection of claims 1, 5, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Kurogawa.

We note that Appellants state on page 6 of the brief that claim 11 stands or falls with claim 10 for the rejection of claims 1, 5, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Sato. We also note that on pages 13 and 14 of the brief, Appellants argue claim 1 separately, but fail to present reasons as to why Appellants consider rejected claims 5 and 10 to be separately patentable from claim 1. For the above reasons we discussed for the rejection based upon Kurogawa, we will also consider Appellants' claims 1, 5, 10 and 11 as standing or falling together as one group and will treat claim 1 as a representative claim of that group for the rejection of claims 1, 5, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Sato.

For the rejection of claims 2, 3, 6, 7, 9, 12 and 13 under 35 U.S.C. § 103 as being unpatentable over Kurogawa and Scharrer, Appellants state on pages 5 and 6 of the brief that claims 9, 12 and 13 are to be treated separately, that claims 2 and 3 stand or fall with claim 1, and that claims 6 and 7 stand or fall with claim 5. We also note that on pages 11 through 13 of the brief, Appellants argue claims 9, 12 and 13 separately. Therefore, we will treat claims 2, 3, 6 and 7, as standing or falling together with claim 1 as being representative and claims 9, 12 and 13 separately.

For the rejection of claims 2, 3, 6, 7, 9, 12 and 13 under 35 U.S.C. § 103 as being unpatentable over Sato and Scharrer, Appellants state on page 6 of the brief that claims 9, 12 and 13 are to be treated separately, that claims 2 and 3 stand or fall with claim 1 and that claims 6 and 7 stand or fall with claim 5. We also note that on pages 14 and 15 of the brief, Appellants argue claims 9, 12 and 13 separately. Therefore, we will treat claims 2, 3, 6 and 7 as standing or falling together with claim 1 as being representative and claims 9, 12 and 13 separately.

In regards to the rejection of claims 1, 5, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Kurogawa, Appellants argue on page 10 of the brief that unlike the teaching of Kurogawa, Appellants' claim 1 is not limited to data bits in the first plurality of storage cells and check bits in the additional plurality of storage cells. Appellants state that claim 1 merely recites undelayed and delayed data, respectively.

Our reviewing court states in *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) that "claims must be interpreted as broadly as their terms reasonably allow." The question before us is not whether Appellants' claim 1 is limited or not limited to data bits in the first plurality of storage

cells and check bits in the additional plurality of storage cells, instead the question before us is whether Appellants' claim language is broad enough in scope to include Kurogawa's memory device.

Appellants' claim 1 recited "a first plurality of storage cells having a predetermined access time for receiving undelayed data" and "at least one additional plurality of storage cells in common array with the first plurality of storage cells and having an access time faster than said predetermined access time for receiving delayed data." Kurogawa teaches on page 9 that Figure 3 shows a memory array 101 having a first plurality of storage cells 201 having a predetermined access time, low-speed memory elements, and at least one additional plurality of storage cells in the common array 101 with the first plurality of storage cells 201 and having an access time faster than said predetermined access time, high-speed elements. Furthermore, Kurogawa teaches on the same page that Figures 3 and 4a show the full write cycle in which the data bits, undelayed data, are written to the first plurality of storage cells 201 without being delayed by a selection circuit. On page 10, Kurogawa teaches that the check bits, delay bits, are written to at least one additional plurality of storage cells 301. We agree that

Kurogawa teaches that the delay bits are check bits. However, the check bits are nonetheless delayed data. Therefore, we find that Kurogawa teaches a first plurality of storage cells and at least one additional plurality of storage cells as recited in Appellants' claim 1.

Appellants further argue that Kurogawa does not teach or suggest a single control means for the memory arrays. Appellants argue that Kurogawa teaches multiple control means in that Kurogawa teaches control means 21 and 11 for memory array 201 and control means 22 and 12 for memory array 301.

We note that Appellants' claim 1 recites "a single control means for: first addressing and storing undelayed data in selected ones of the first plurality of storage cells, and later addressing and storing delayed data in selected ones of the at least one additional plurality of storage cells." Upon reviewing this claim language, we do not find that Appellants' claim 1 precludes two separate circuits within the single control means. In other words, a single control means can be properly construed as a separate circuit with the single control means for first addressing and storing undelayed data in selected ones of the first plurality of storage cells and another separate circuit within the single control means for later addressing and storing

delayed data in selected ones of at least one additional plurality of storage cells. Furthermore, we note that the claim does not require that the single control means be placed on a single substrate or arranged on a chip in one location.

In fact, Appellants' specification teaches that the single control means includes separate circuits for performing these functions in that data bits and check bits are addressed and stored by separate circuits. On pages 26 and 27 of the specification, Appellants disclose that to cause the storage of the data bits as soon as they are valid, it is necessary to make modifications to the circuitry illustrated in Figure 2. Appellants disclose that Figure 14 is an illustration of the modified Figure 2 circuitry. Figure 14 shows that driver 64 is now connected to receive the RAS and RASN signals over the indicated lines, the RASN line including an inverter 101. The modified circuitry illustrated in Figure 14 will thus cause all data bits to be directed to the DRAM storage cells while the check bits are being calculated by logic circuits labeled 30S1-30S9 (Figure 1). The check bits will then be sent to the DRAM cells as soon as they are calculated. Furthermore, Figures 13 and 14 show that there are separate circuitry connecting the data bits to data cells and check bits to check bit cells in the DRAM. Thus, we

agree that Appellants' specification discloses a single control means but also clearly discloses that there are separate circuitry within the single control means for addressing and storing data bits and for addressing and storing check bits in the DRAM.

Kurogawa teaches on page 9 that Figures 3 and 4 show a control means 21 for first addressing and storing undelayed data, Din, in selected ones of the first plurality of storage cells, first memory array 201. Kurogawa teaches on page 10 that Figures 3 and 4 show a control means 22 for then addressing and storing delay data, D'in, in selected ones of at least one additional plurality of storage cells, second memory array 301.

We note that not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. *See In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968); *In re Shepard*, 319 F.2d 194, 197, 138 USPQ 148, 150 (CCPA 1963); and *In re Sernaker*, 702 F.2d 989, 994, 217 USPQ 1, 5 (Fed. Cir. 1983). Skill in the art is presumed. *See In re Sovish*, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). In *Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1090, 37 USPQ2d 1237, 1240-41 (Fed. Cir. 1995), our reviewing court points out that motivation or teaching for

a person of ordinary skill in the art to make a modification to a reference does not require an explicit teaching but may be implied in view of the reference and the general knowledge of one skilled in the art. The Federal Circuit also noted that we can presume that the person of ordinary skill in the art would have carefully examined all of the teachings of the reference and that the person of ordinary skill in the art would use these teachings to solve the problem recognized by the prior art.

The only distinction between Appellants' claim 1 is that Kurogawa did not draw a box around the control means 21 and 22 and label it as a single control means. We note that Kurogawa did draw a single box around the two memories 201 and 301 and label it a single memory 101 even though the two memories are made up of different circuitry. Kurogawa's labeling of the memory demonstrates that it is desirable to label circuitry on the system level as opposed to the circuitry level for better understanding of the invention. Therefore, it would have been obvious to one of ordinary skill in the art to draw a single box around the Kurogawa control circuitry and label the box as a single control means to emphasize the system control function of the control circuitry within the box in order to obtain Appellants' invention as recited in claim 1.

In regards to claims 2, 3, 6, 7, 9, 12 and 13 under 35 U.S.C. § 103 as being unpatentable over Kurogawa and Scharrer, Appellants argue that claim 9 recites a single control means and that Scharrer adds nothing in the rejection of claim 9. We agree. However, for the above same reasons, we find that it would have been obvious to one of ordinary skill in the art in view of the Kurogawa teachings to obtain a single control means as claimed by Appellants' claims. Appellants further argue that claims 12 and 13 recite a faster memory cell in the form of a transistor with wider source and drain diffusion regions. Appellants argue that although Scharrer states in column 6, lines 65-66, "for a given size transistor, the Write speed will be increased," Scharrer makes no reference in the cited portion to a particular size transistor, let alone increasing the size thereof.

Upon a closer inspection of Scharrer, we find that in column 1, lines 22-40, Scharrer teaches that in bipolar technology, the transistors have a higher transconductance, thus providing inherently faster operation due to lower source impedance. However, Scharrer is not concerned with providing faster speed but reducing power consumption and thereby allows for small transistors. See column 1, lines 57-63. In column 2,

lines 29-36, Scharrer teaches that current is reduced and thereby power consumption is reduced by isolating the output of the CMOS inverter in a CMOS latch when writing to the memory cells such that only the high impedance input is driven. Scharrer further teaches that once the power consumption is reduced then this allows for smaller size transistors.

In column 6, lines 22-49, Scharrer further teaches the CMOS latch operation. Scharrer points out the only purpose of the Write circuity is not to pull the driven sense node down when changing from a high logic state to a low logic state, but rather to turn off the opposite side N-channel transistor. When pulling the driven sense node in a conventional CMOS latch from a high state to a low state, the opposite situation occurs, in that current is being pulled through the P-channel transistor with the P-channel transistor requiring a larger size device to handle this additional current. Thus, Scharrer is teaching that because of the additional power requirements the transistor is required to be larger.

In column 6, lines 50-66, Scharrer discloses a system which is able to use a smaller transistor by preventing the additional current being drawn through one of the P-channel transistors. Scharrer teaches that the Write Select transistor

104 disconnects the gates of one complimentary pair of transistors from the opposite sense node during the Write Operation. Scharrer does teach that a same size transistor using the Scharrer system will increase write speed. However, Scharrer does not teach that the increased writing speed is due to increasing the width of the source and drain diffusion regions as recited in Appellants' claims 12 and 13. We simply do not have any evidence before us that supports the Examiner's rationale that an increased writing speed in a memory cell is accomplished by increasing the width of the source and drain diffusion regions.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a *prima facie* case. *In re Knapp-Monarch Co.*, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); *In re Cofer*, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Therefore, we will not sustain the Examiner's rejection of claims 12 and 13.

In regard to the rejection of claims 1, 5, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Sato, we note that Sato teaches all of the claim limitations of Appellants'

claim 1 except that Sato did not draw a box around the control circuitry and label it a single control means. For the same rationale above, we find that it would have been obvious for one of ordinary skill in the art in view of the Sato teachings to obtain Appellants' invention as recited in claim 1, and thereby claims 3, 10 and 11. In regard to the rejection of claims 2, 3, 6, 7, 9, 12 and 13 under 35 U.S.C. § 103 as being unpatentable over Sato and Scharrer, we find using the above rationale that it would have been obvious to one of ordinary skill in the art in view of the teachings of Sato to obtain Appellants' invention as recited in claims 2, 3, 6, 7 and 9. However, as shown above, we fail to find that Scharrer teaches the claimed limitation as recited in claims 12 and 13, and thereby we will not sustain the Examiner's rejection of claims 12 and 13 as being unpatentable over Sato and Scharrer under 35 U.S.C. § 103.

In view of the foregoing, we will sustain the decision of the Examiner rejecting claims 1 through 3, 5 through 7, and 9 through 11 as being directed to subject matter that would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103. However, we will not sustain the decision of the Examiner rejecting claims 12 and 13 as being directed to subject matter that would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

RAYMOND F. CARDILLO, JR.
Administrative Patent Judge

LEE E. BARRETT
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. 95-2675
Application 07/785,625

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Japanese 57-143800

Code PTO 93-3742

Japanese Kokoku Patent Application
Sho 57[1982]-143800

MEMORY DEVICE

UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. SEPTEMBER 1993
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JAPANESE PATENT OFFICE

PATENT JOURNAL

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MEMORY DEVICE
[Kioku Sochi]

Inventor: Hidetsune Kurogawa

Applicant: NEC Corp.

[There are no amendments to this patent.]

Claim

A type of memory device characterized by the following facts: the memory device contains the following parts: a memory array which stores the data bits and the check bits, a check bit generating means which generates check bits from the write information, a means which performs error-detection and correction for the output information and which sends the corrected read information, and a means which generates the check bits from the read information in the partial write operations and uses them to replace the check bits stored in the aforementioned memory array; in this memory device for performing read, full write, and partial write operation, the aforementioned memory array consists of a first memory array which contains the data bits and a second memory array which contains the check bits; the aforementioned second memory array is made of memory elements with a speed higher than that of the aforementioned first memory array; control is executed appropriately for the memory device to ensure that in the case of the partial write operation, in the aforementioned first memory array, the write portion performs read/write operations, and the nonwrite portion performs the read operation; on the other hand, the aforementioned second memory array writes the check bits generated from the read information and performs the read-modify write operation.

Detailed explanation of the invention

This invention concerns a type of memory device. More

specifically, this invention concerns a configuration which enables shortening of the partial write operation cycle time for the memory device having the partial write operation function.

In recent years, significant progress has been achieved in the performance of computers. This progress can be mainly attributed to the advance of the technology, particularly the increase in the operating speed of the logic elements and the increase in the operating speed of the central processing unit (referred to as CPU hereinafter) made possible by increasing the level of integration. On the other hand, for the main memory device (referred to as MEM hereinafter), although the level of integration has been increased by about a factor of four in the past 2-3 years for the dynamic MOS RAM used in almost all of MEMs there nevertheless has been no significant improvement in performance (cycle time, access time) in several years. Consecequently, the gap between the performance of the CPU and the performance of the MEM has widened. As this gap widens, the requirements raised by the CPU cannot be well met by the MEM. Many methods have been proposed to reduce this gap. A well-known example is cache memory, which can be placed in the CPU to cover the delay in the access time of MEM (as compared to what required). Cache memory is a partial copy of MEM. When the CPU loads commands and operands (referred to as data hereinafter), if the data needed is in cache, the data can be loaded directly from cache without the need to access the MEM. It is well known that when the cache memory capacity is increased, the probability of finding of the data needed by CPU in cache, that is, the hit rate, can be improved. Consecequently, the requirement for the number of access cycles to the MEM in the load operation, that

is, the requirement for the throughput of the MEM, can be relaxed by means of increasing the cache volume. On the other hand, in the case when CPU executes storage, that is, the write operation, the write-through method is adopted, and the number of accesses to MEM is different from that of the case of the load operation.

In the write-through method, when the address to be stored is registered in cache in the storage operation, the [address] is stored in both cache and MEM. On the other hand, in the write-swap method, [the address] is stored only in cache but not in MEM. For the multi-processor comprising of multiple CPUs, the former method is preferred in consideration of the advantage of matched processing capability of the cache. Consecequently, the write-through method is adopted in ultra-large systems.

However, as can be seen from the above explanation, in the case of the write-through method, when the storage operation is performed, regardless of whether or not the cache is hit, accessing always extends to MEM. Although the ratio of the number of stores to loads generated in the CPU depends on the combination of the commands to be executed and thus cannot be generally defined, as cache capacity is increased, access to MEM tends to have a higher number of stores than loads. In addition, in the case of the store operation, there are both partial stores and full stores, and usually the number of partial stores (or, partial write, which is more often used in the case of MEM) with access to the MEM is higher. Consequently, in order to increase the throughput of the MEM, that is, the number of access cycles that can be processed by MEM per unit time, it is preferred that the partial write operation cycle time be reduced.

However, for the MEM of the prior art, the partial write operation cycle time is usually nearly twice the read cycle time or the full write cycle time, and multiple CPUs share the MEM. In particular, when the application efficiency of MEM is high, the system performance is often restrained by the throughput of MEM as the partial write operation cycle time now becomes the crucial factor. In the conventional MEM, in order to increase the throughput, efforts are made to increase the speed of the partial write operation by using high-speed elements for all of the memory elements. However, although an overall higher speed can be realized, the cost is nevertheless significantly increased. Another disadvantage of the conventional method is that since the partial write operation cycle time in the MEM is about twice the full write and read cycle time, management of the MEM when busy becomes complicated, and much hardware for control is needed.

The aforementioned viewpoints may be further explained with reference to Figures 1 and 2. Figure 1 is a block diagram of a conventional type of this kind of memory device. Figure 2 is a timing diagram for illustrating its operation. That is, in this configuration, memory array (100) is made of memory array (200) for data bits and memory array (300) for check bits. The memory elements that form memory array (200) and the memory elements that form memory array (300) are of the same type.

In the full write operation, for write information WD, only the data bits are sent through a selection circuit (30) to memory array (200) for data bits. At the same time, Hamming check bits are generated by a Hamming generation circuit (40). The generated Hamming check bits are sent to memory array (300) for

the check bits. Then, under control by clock CE and write/read control signal W/R sent from control circuit (20), the data bits and the check bits are stored, respectively, from memory array (200) for data bits and memory array (300) for check bits to the memory element with address provided by address control circuit (10). Said clock CE and write/read control signal W/R are sent to both memory array (200) for data bits and memory array (300) for check bits from control circuit (20). Consequently, in the full write cycle shown in Figure 2(a), the input information Din is stored in said two memory arrays (100) and (200) under control of the write/read control signal W/R. Here, the full write operation refers to the conventional write operation, it bears this name here only to make a distinction with the partial write operation to be explained later. That is, in the full write operation, only the write operation is performed for said memory arrays (200) and (300), without any relationship to the information stored before. However, in the case of the partial write operation to be discussed later, the memory array performs a read-modify write. In the read-modify write operation, the stored information is read, modified, and reloaded into its original address.

Then, in the read operation, as shown in Figure 2(b), address information AD is sent to said memory array (200) for data bits and memory array (300) for check bits; from the corresponding address, the memory contents are output as output information Dout. In this case, input information Din becomes irrelevant. Figure 2(b) shows a timing diagram for clock CE, address information AD, and output information Dout in the read cycle. For output information Dout, by means of error detection

circuit (50) shown in Figure 1, the error is detected and corrected by an error correction circuit (60), followed by outputting read information RD to the device as the source of the request.

In the case of the partial write operation, memory array (100) performs the read-modify write operation. That is, just as in the aforementioned read operation, error-corrected read information RD is read and sent to a selection circuit (30); at selection circuit (30), only the reloaded portion is swapped with write information WD sent from the outside so as to form new write information; then, in the same way as in the aforementioned write operation, the data bits are loaded into memory array (200) for data bits, and the Hamming check bits are loaded into memory array (300) for check bits. Figure 2(c) shows the timing diagram of clock CE, address information AD, output information Dout, input information Din, and write/read control signal W/R in the partial write operation. As can be understood with reference to this figure, in the conventional device, the cycle time of the partial write operation is almost equal to the sum of the read cycle time and the full write cycle time. In other words, since the read cycle time is usually set equal to the cycle time of the full write cycle--suppose it is Tc--the cycle time of the partial write operation becomes about 2Tc.

The number of access cycles from CPU to MEM depends on the program to be executed and the design of the cache, and thus cannot be simply predicted. However, in some cases, it may be about twice the sum of the number of partial write cycles and the number of full write cycles, instead of the number of read cycles. Since the number of the partial write operations is

usually greater than that of the full write operations, in order to improve the throughput of MEM, it is preferred that the speed of the partial write operation be increased. On the other hand, in the conventional MEM, as pointed out in the above, the partial write operation is slow. In order to increase the speed of the partial write operation, the only option is to use expensive, high-speed memory elements so as to increase the overall speed of the operation cycle.

The purpose of this invention is to solve the aforementioned problems of the conventional methods by providing a type of memory device which has a high speed and is relatively inexpensive.

That is, this invention provides a type of memory device characterized by the following facts: the memory device contains the following parts: a memory array which stores the data bits and the check bits, a check bit generating means which generates check bits from the write information, a means which performs error-detection and correction for the output information and which sends the corrected read information, and a means which generates the check bits from the read information in the partial write operation and uses them to replace the check bits stored in the aforementioned memory array; in this memory device for performing read, full write, and partial write operations, the aforementioned memory array consists of a first memory array which contains the data bits and a second memory array which contains the check bits; the aforementioned second memory array is made of memory elements with a speed higher than that of the aforementioned first memory array; control is executed appropriately for the memory device to ensure that in the case of

the partial write operation, in the aforementioned first memory array, the write portion performs read/write operations, and the nonwrite portion performs the read operation; on the other hand, the aforementioned second memory array writes the check bits generated from the read information and performs the read-modify write operation.

In the following, this invention will be explained in more detail with reference to application examples illustrated by figures.

Figure 3 is a block diagram illustrating an application example of this invention. Figure 4 is a timing diagram illustrating the operation in this application example.

As shown in Figure 3, memory array (101) is made of first memory array (201) for data bits made of low-speed memory elements and second memory array (301) for check bits made of high-speed memory elements. For example, for first memory array (201), 64 K dynamic MOS-RAM (standard properties: access time in the range of 150-200 nsec, cycle time about 300 nsec) may be used as the memory elements; for second memory array (301), 16 K static MOS-RAM (standard properties: both cycle time and access time about 50-70 nsec) may be used as the memory elements.

As shown in Figures 3 and 4(a), in the full write cycle, for first memory array (201), input information Din is loaded into the address assigned by address control circuit (21) under control of the read/write control signal W/R sent from the address control circuit (21). As the input information Din, the data bits of write information WD from the outside are sent directly (without going through a selection circuit as in the aforementioned conventional example). On the other hand, for

second memory array (301), write information WD from the outside is selected and kept by means of a selection circuit (31), and the Hamming bits generated by Hamming generation circuit (41) is provided as input information D'in. As shown in Figure 4(a), in second memory array (301), the write operation is started by means of clock CE_2 delayed by a time Tw under control of clock CE_1 output from control circuit (21), and input information D'in is loaded by means of write/read control signal W/R. That is, the write operation of second memory array (301) is started after a delay of Tw from start of the write operation of first memory array (201). However, since second memory array (301) can perform high-speed operations, the write operation can be completed in a short period of time.

Then, in the read cycle operation, just as in the above, the operation of second memory array (301) is started after a delay of Tw from start of the write operation of first memory array (201). This delay time Tw should be set in an appropriate range to ensure that output information D'out is not delayed as compared to output information Dout of first memory array (201) since second memory array (301) has a high speed of operation. Both output information Dout of first memory array (201) and output information D'out of second memory array (301) are input to an error detection circuit (51) for error detection; and read information RD is obtained after error correction by error correction circuit (61).

Then, in the partial write operation, under control of control circuit (21), the read/write operation is carried out in the data reloading portion of first memory array (201), and the

read operation is carried out for the portion without reloading. On the other hand, under control of control circuit (22), second memory array (301) performs the read-modify write operation. That is, when the memory elements of first memory array (201) perform the read/write operation, the contents stored in the address before can be output at the same time of the write operation. In other words, for the memory elements in first memory array (201), even in the case of the write operation, the contents stored at the address before can be read in the same access time as the read operation. This function can be realized by means of the dynamic MOS-RAM which defines the read/write cycle. In addition, there are also elements for which the output is changed from the contents stored before to the write data when the write enable signal (the write assigning signal) activates the write state. For these types of elements, only a little time is needed to input the write enable signal after the read data is fully established. These types of elements may also be used. In this application example, the elements which perform a read at the same time as a write are the former type a used.
Consequently, while write information WD is newly loaded into the reloading portion in first memory array (201), just as in the read cycle, output information Dout formed by reading of the data bits are sent together with the Hamming check bits read from second memory array (301) to error detection circuit (51). In addition, read information RD corrected by error correction circuit (61) is obtained. The portion in said read information RD corresponding to the write data bits in first memory array (201) is replaced by write information WD at selection circuit (31), and is then sent to Hamming bit generation circuit (41);

Hamming bit generation circuit (41) then generates the new Hamming bits, which are sent to second memory array (301). These bits are loaded in said second memory array (301). The operation of said second memory array (301) is started by clock CE_2 delayed by a delay time Tp1 from clock CE_1, as shown in Figure 4(c). However, reading of the check bits, that is, output of output information D'out, is carried out at the same time as output information Dout from memory array (201). The corrected check bits generated from read information RD as explained above are input as input information D'in, and they are loaded by means of write/read signal W/R'. The operation end time is delayed by Tp_2 from the operation start time of the next cycle of first memory array (201). In this application example, the aforementioned delay time Tp_2 is shorter than the aforementioned delay times T_W, T_R and T_{p1}. In addition, the cycle times for write, read and read-modify write of second memory array (301) are set shorter than the cycle times of write, read and read-modify write of first memory array (201). Consequently, in this application example, the cycle time and access time are determined solely by the operating speed of first memory array (201). For example, if first memory array (201) has the same cycle time for its read cycle, write cycle and read-modify write cycle, it is possible to ensure the same cycle time for the read operation, full write operation, and partial write operation in this application example. As a result, the partial write operation cycle time can be halved as compared with that of the conventional case. This is a significant effect.

In the conventional device, in order to make the partial write operation cycle time as short as in this application example, all of the memory elements in the memory array (100) shown in Figure 1 must be high-speed elements. The high-speed elements not only are more expensive, but they also have a low level of integration. Consequently, with the conventional method the size and cost of the device must increase to increase the operating speed.

This invention, however, is not limited to the aforementioned application examples. It allows appropriate changes in the method of applying the control signal of the memory array corresponding to the type of the elements used.

In conclusion, in this invention, both high-speed elements and low-speed elements are used in the memory array, and only the memory array for the check bits make use of the high-speed elements alone; the start time of the operation of the memory array for the check bits is delayed slightly from the start time of the operation of the memory array for the data bits; and in the case of the partial write operation, the aforementioned delay time of the end of operation of the memory array for check bits is within the range of the aforementioned delay time of start of operation. With this configuration, the cycle time of the partial write operation can be significantly shortened as compared to that of the conventional method. Consequently, for the general system adopting the memory device of this invention, the overall operation is faster and the efficiency is increased significantly. The effects are very significant. In addition, in this invention, since only a portion of the elements need be high-speed elements, the cost can be cut.

Brief explanation of the figures

Figure 1 is a block diagram illustrating an example of the conventional memory device. Figure 2 is a timing diagram illustrating the operation in the aforementioned conventional device. Figure 2(a) shows the operation in the full write cycle. Figure 2(b) shows the operation in the read cycle. Figure 2(c) shows the operation in the partial write cycle. Figure 3 is a block diagram of an application example of this invention. Figure 4 is a timing diagram illustrating the operation in the aforementioned conventional device. Figure 4(a) shows the operation in the full write cycle. Figure 4(b) shows the operation in the read cycle. Figure 4(c) shows the operation in the partial write cycle.

10-12, address control circuit
20-22, control circuit
30, 31, selection circuit
40, 41, Hamming generation circuit
50, 51, error detection circuit
60, 61, error correction circuit
100,101,200,300, memory array
201, first memory array
301, second memory array

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SEMICONDUCTOR MEMORY DEVICE

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SEMICONDUCTOR MEMORY DEVICE
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Claims

1. A type of semiconductor memory device characterized by the fact that it consists of an ECC circuit which receives input data made of multiple bits and forms the prescribed check bits, a first memory array which stores the aforementioned input data and has a relatively long access time, and a second memory array which stores the aforementioned check bits and has a relatively short access time.

2. The semiconductor memory device described in Claim 1 characterized by the fact that the aforementioned first memory array is made of dynamic memory cells, and the aforementioned second memory array is made of static memory cells.

3. The semiconductor memory device described in Claim 1 or 2 characterized by the fact that the aforementioned semiconductor memory device also has address decoders corresponding to the aforementioned first and second memory arrays, respectively.

4. The semiconductor memory device described in Claim 1, 2, or 3 characterized by the fact that the aforementioned ECC circuit, the aforementioned first and second memory arrays, and the aforementioned address decoders are all formed on a single semiconductor substrate.

Detailed explanation of the invention

Industrial application field

This invention concerns a type of semiconductor memory device. It concerns a technology which may be used effectively

in manufacturing RAM (Random Access Memory) containing ECC circuit (Error Correction Code circuit), etc.

Prior art

The ECC method can be used to detect and correct the errors in the transmitted data by annexing check bits formed according to a prescribed algorithm. There are RAM and other semiconductor memory devices which add the aforementioned check bits to the stored data. The RAM or other semiconductor memory device of this type has an ECC circuit which contains a check bit generating circuit which can form the check bits when the data are written, and an error correcting circuit which checks the state of the data and makes corresponding changes in the case of the data read operation. The aforementioned RAM and other semiconductor memory devices may form the memory units in computers and other digital processing equipment.

As an example, the ECC method is described in "LSI Handbook," p. 527, published on November 30, 1984, by Ohm Co.

Problems to be solved by the invention

However, the aforementioned semiconductor memory device, such as RAM, containing the ECC circuit has the following disadvantages. In the RAM or other semiconductor memory device, the check bits formed corresponding to the input data are stored in the prescribed bits pre-allocated in the memory array which also stores the input data. In other words, the input data and the corresponding check bits are stored in the same memory array.

On the other hand, the aforementioned ECC circuit for generating the check bits has a check bit generating circuit containing an exclusive-OR logic circuit for receiving a prescribed amount of input data. Consequently, when the bit number of the input data is as large as 32 or 64, the number of bits input to the aforementioned exclusive-OR circuit is increased, and the corresponding time needed for forming the check bits becomes longer.

Consequently, the access time of the RAM or other semiconductor memory device containing the aforementioned ECC circuit is equal to the sum of the access time of the memory array that forms the semiconductor memory device and the time of operation of the check bit generating circuit. It thus becomes longer. As a result, for the digital processing equipment containing the memory unit made of the aforementioned RAM or other semiconductor memory device, the cycle time becomes longer, and the processing ability is worsened.

The purpose of this invention is to solve the aforementioned problems of the conventional methods by providing a type of semiconductor memory device characterized by the fact that the access time can be reduced when the data are written into the RAM or other semiconductor memory device containing the ECC circuit. Another purpose of this invention is to improve the processibility of the digital processing equipment containing the aforementioned RAM or other semiconductor memory device.

The aforementioned purposes and other purposes of this invention will be explained in the following with reference to annexed figures.

Means for solving the problems

The following is a brief explanation of the typical method of the invention disclosed in this patent application. That is, this invention provides a type of semiconductor memory device, such as RAM, etc. characterized by the fact that it consists of an ECC circuit which receives input data in multiple bit form and generates the prescribed check bits, a memory array which stores the aforementioned input data and has a relatively long access time, and a memory array which stores the aforementioned check bits and has a relatively short access time.

Functions

By means of the aforementioned configuration, the sum of the access time of the memory array that contains the check bits and the operating time needed for the ECC circuit to form the check bits is almost identical to the access time of the memory array which stores the input data. As a result, the access time can be significantly reduced in the write operation to RAM or other semiconductor memory device containing the ECC circuit. In this way, the cycle time of the digital processing equipment containing the RAM or other semiconductor memory device as the memory unit can be increased, and the processibility can also be improved.

Application examples

Figure 1 is a block diagram of an application example of memory unit MU made of the RAM (Random Access Memory) of this invention. There is no particular limitation on the manufacturing technology for the circuit elements forming the various blocks shown in this figure, and any manufacturing technology of the semiconductor IC may be adopted in this case. However, the elements should all be formed on a single semiconductor substrate.

There is no particular limitation on the type of the memory unit MU in this application example. The memory unit should nevertheless be contained in computer or other digital processing equipment. Although there is no particular limitation on memory unit MU, it should be coupled to the system bus of the digital processing equipment via a memory control unit (not shown in the figure). Memory unit MU contains an ECC circuit comprising check bit generating circuit CG and an error correction circuit comprising a syndrome generating circuit SG and a data correcting circuit DC. In this application example, the data which is input/output to/from memory unit MU via a system bus and a memory control unit has a 32-bit configuration. The ECC circuit adopts the single-error-correction/double-error-detection method, and it annexes check bits in 7-bit format. That is, in this application example, there are 39 bits for the sum of the stored data. In the read operation, a 1-bit error generated in the memory data is

detected and corrected. However, when a 2-bit error occurs, the error is detected but not corrected. When an error is detected in the read data, a low-level error detection signal ED is sent from memory unit MU to the memory control unit.

As will be explained later, the memory unit MU used in this application example contains memory array MARYD (the first memory array) made of dynamic memory cells, and memory array MARYS (the second memory array) made of static memory cells. Memory array MARYD forms data memory DM which stores the aforementioned 32-bit input/output data, while memory array MARYS forms check bit memory CM which stores the aforementioned 7-bit check bits. In this application example, the access time of check bit memory CM is set as the time derived by subtracting the operation time of check bit generation circuit CG of the ECC circuit from the access time of data memory DM. In this way, the overall access time of memory unit MU depends only on the access time of data memory DM and is independent of the operation time of the ECC circuit. Consequently, the operation speed can be increased.

As shown in Figure 1, memory array MARYD of data memory DM consists of m + 1 word lines arranged in the vertical direction of this figure, 32 x (n + 1) groups of complementary data lines arranged in the horizontal direction, and 32 x (m + 1) x (n x 1) dynamic memory cells arranged in grid form at the intersections between these word lines and the complementary data lines.

The word lines that form memory array MARYD are coupled to X address decoder XADD, and are set in the alternative high-level selected state.

In the X address decorder XADD, from X-address buffer XAB (to be explained later), (i + 1)-bit complementary internal

address signal ax0-axi (in this case, for example, noninverted internal address signal ax0 and inverted internal address signal ax0 are combined and represented by the complementary internal address signal ax0; the same in the following). In addition, timing signal ϕxd is supplied from the timing generation circuit TG (to be explained later).

Since the aforementioned timing signal ϕxd is set to the high level, X-address decoder XADD is set selectively to the operating state. In this operating state, X-address decoder XADD decodes the aforementioned complementary internal address signals ax0-axi, and the corresponding word line of memory array MARYD is alternately set to the high-level selective state.

X-address buffer XAB receives and holds X-address signals AX0-Axi fed through external terminals AX0-AXi. Based on these X-address signals AX0-AXi, said complementary internal address signals ax0-axi are formed and fed to said X-address decoder XADD. Complementary internal address signals ax0-axi are also sent to X-address decoder XADS of check bit memory CM (to be explained later).

The complementary data lines that form memory array MARYD are coupled to the corresponding unit amplifier circuit of sense amplifier SA on the one hand, and the corresponding switch MOSFET pair of column switch CSWD on the other.

Sense amplifier SA contains 32 x (n + 1) unit amplifier circuits corresponding to the complementary data lines of memory array MARYD. Timing signal ϕpa is at once sent from timing generation circuit TG to these unit amplifier circuits.

Since said timing signal ϕpa is set at the high level, each unit amplifier circuit of sense amplifier SA is selectively set

to the operating state. In this operating state, the various unit amplifier circuits of sense amplifier SA amplify the low small amplitude read signals output from the 32 x (n + 1) memory cells coupled to the selected word lines of memory array MARYD via the corresponding complementary data lines, and form high-level or low-level binary read signals.

Column switch CSWD contains 32 x (n + 1) groups of switch MOSFET pairs corresponding to the complementary data line of said memory array MARYD. On one side, these switch MOSFET pairs are coupled to the corresponding complementary data lines of memory array MARYD. On the other hand, they are coupled in 32 groups to the corresponding complementary common data lines CDD0-CDD31 (here, for example, noninverted signal line CDD0 and inverted signal line CDD0 are represented together as complementary common data line CDD0; same in the following.) The gates of the switch MOSFET pairs that form column switch CSWD are commonly coupled for every 32 groups, and corresponding data line selection signals YD0-YDn are fed, respectively, from Y-address decoder YADD.

Since corresponding data line selection signals YD0-YDn are set alternately to the high level, the corresponding 32 groups of switch MOSFET pairs of column switch CSWD all turn ON. Consequently, 32 groups of complementary data lines are selected from memory array MARYD, and are connected to said corresponding complementary common data lines CDD0-CDD31.

From Y-address buffer YAB (to be explained later), (j + 1)-bit complementary internal address signals ay0-ayj are fed to Y-address decoder YADD. In addition, timing signal ϕyd is sent from timing generation circuit TG.

Since said timing signal ϕyd is set to the high level, Y-address decoder YADD is set selectively to the operating state. In this operating state, Y-address decoder YADD decodes said complementary internal address signals ayo-ayj, and the corresponding data line selection signals YD0-YDn are alternately set to the high level.

Y-address buffer YAB fetches and holds Y-address signals AY0-AYj fed via external terminals AY0-AYi. Based on these Y-address signals AY0-AYj, said complementary internal address signals ay0-ayj are formed, and are fed to said Y-address decoder YADD. Complementary internal address signals ay0-ayj are also sent to Y-address decoder YADS of check bit memory CM (to be explained later).

Complementary common data lines CDD0-CDD31 selectively connected to the 32 groups of complementary data lines assigned by memory array MARYD are coupled to the output terminals of the corresponding unit circuits of write amplifier WAD, respectively, and they are also coupled to the input terminals of the corresponding unit circuits of read amplifier RAD.

Write amplifier WAD has 32 unit circuits corresponding to said complementary common data lines CDD0-CDD31. From data input buffer DIB to be explained later, corresponding internal input data di0-di31 are fed to the input terminals of these unit circuits, respectively. On the other hand, from timing generation circuit TG, timing signal ϕwd is at once fed to these unit circuits.

Since said timing signal ϕwd is set to the high level, each unit circuit of write amplifier WAD is set selectively to the operating state. In this operating state, the various unit

circuits of write amplifier WAD send corresponding internal input data di0-di31 as the complementary write signals to corresponding complementary common data lines CDD0-CDD31.

Via data input terminals D0-D31, data input buffer DIB sends the 32-bit write data as said internal input data di0-di31 to corresponding unit circuits of said write amplifier WAD. This internal input data di0-di31 is also fed to the ECC circuit (to be explained later).

Read amplifier RAD has 32 unit circuits corresponding to the aforementioned complementary common data lines CDD0-CDD31. The output signals of these unit circuits are sent as read data dr0-dr31 to the ECC circuit. In addition, timing signal ϕrd is sent at once from timing generation circuit TG to all these unit circuits.

Since said timing signal ϕrd is set to the high level, the various unit circuits of read amplifier RAD is set selectively to the operating state. In this operating state, the various unit circuits of read amplifier RAD make further amplify the binary read signal transmitted from the selected memory cell of memory array MARYD to corresponding complementary common data lines CDD0-CDD31, and then send them as said read data dr0-dr31 to the ECC circuit.

On the other hand, memory array MARYS of check bit memory CM consists of m + 1 word lines arranged in the vertical direction of the figure, 32 x 7 groups of complementary data lines set in the horizontal direction, and 7 x (m + 1) x (n + 1) static memory cells arranged in grid form at the intersections between the aforementioned word lines and complementary data lines.

The word lines that form memory array MARYS are coupled to X-address decoder XADS, and are set alternately to the high-level selective state.

Said complementary internal address signals ax0-axi are fed from X-address buffer XAB to X-address decoder XADS, and timing signal ϕxs is fed from timing generation circuit TG.

Since said timing signal ϕxs is set to the high level, X-address decoder XADS is selectively set to the operating state. In this operating state, X-address decoder XADS decodes said complementary internal address signals ax0-axi, and the corresponding word lines of memory array MARYS are alternately set to the high-level selected state.

The complementary data lines forming memory array MARYS are coupled to corresponding switch MOSFET pairs of column switch CSWS.

Column switch CSWS contains 7 x (n + 1) groups of switch MOSFET pairs which correspond to the complementary data lines of the aforementioned memory array MARYS. On the one hand, these switch MOSFET pairs are coupled to the corresponding complementary data lines of memory array MARYS. On the other hand, they are commonly coupled, in 7 groups, to corresponding complementary common data lines CDS0-CDS6. The gates of the switch MOSFET pairs that form column switch CSWS are coupled to each other in sequence to form 7 groups, and corresponding data line selection signals YS0-YSn are fed respectively from Y-address decoder YADS.

Since corresponding data line selection signals YS0-YSn are alternately set to the high level, the corresponding 7 groups of switch MOSFET pairs of column switch CSWS are turned ON at the

same time. In this way, the 7 groups of complementary data lines are selected from memory array MARYS and connected to corresponding said complementary common data lines CDS0-CDS6.

From Y-address buffer YAB, said complementary internal address signals ay0-ayi are sent to Y-address decoder YADS, and timing signal ϕys is fed from timing generation circuit TG.

Since said timing signal ϕys is set to the high level, Y-address decoder YADS is selectively set to the operating state. In this operating state, Y-address decoder YADS decodes said complementary internal address signals ay0-ayj, and the corresponding said data line selection signals YS0-YSn are alternately set to the high level.

Complementary common data lines CDS0-CDS6, which are selectively connected to the assigned 7 groups of complementary data lines of memory array MARYS are coupled to the respective output terminals of write amplifier WAS and also to the internal terminals of the corresponding unit circuits of read amplifier RAS;

Write amplifier WAS contains 7 unit circuits corresponding to said complementary common data lines CDS0-CDS6. The corresponding internal write check bits cw0-cw6 are fed from the ECC circuit (to be explained later) to the respective input terminals of these unit circuits. In addition, timing signal ϕws is fed at once from timing generation circuit TG to these unit circuits.

Since said timing signal ϕws is set to the high level, the various unit circuits of write amplifier WAS are set selectively to the operating state. In this operating state, the various unit circuits of write amplifier WAS send the corresponding said

internal write check bits cw0-cw6 as complementary write signal to corresponding complementary common data lines CDS0-CDS6.

Read amplifier RAS contains 7 unit circuits corresponding to said complementary common data lines CDS0-CDS6. The output signals of these unit circuits are sent as read check bits cr0-cr6 to the ECC circuit (to be explained later). In addition, timing signal ϕrs is sent at once from timing generation circuit TG to these unit circuits.

Since said timing signal ϕrs is set to the high level, the various unit circuits of read amplifier RAS are selectively set to the operating state. In this operating state, the various unit circuits of read amplifier RAS amplify the read signal transmitted from the selected memory cell of memory array MARYS to the corresponding complementary common data lines CDS0-CDS6, and send them as said read check bits cr0-cr6 to the ECC circuit.

Internal input data di0-di31 are sent from said data input buffer DIB to the ECC circuit, and internal read data dr0-dr31 are sent from said read amplifier RAD to the ECC circuit. Also sent to the ECC circuit are internal read check bits cr0-cr6 from said read amplifier RAS and internal control signal wm from timing generation circuit TG. Since memory unit MU is set to the write operation mode, this internal control signal wm is selectively set to the high level.

When memory unit MU is set to the write operation mode and when said internal control signal wm is set to the high level, the ECC circuit acts as a check bit generating circuit. In this case, based on internal input data di0-di31 fed from data input buffer DIB, the ECC circuit forms 7-bit check bits and sends them as internal write check bits cw0-cw6 to said write amplifier WAS.

On the other hand, when memory unit MU is set to the read operation mode and said internal control signal wm is set to the low level, the ECC circuit acts as an error correcting circuit. In this case, based on internal read data dr0-dr31 fed from read amplifier RAD and internal read check bits cr0-cr6 fed from read amplifier RAS, the ECC circuit forms syndromes s0-s6, and checks the state of the read data to see if they are normal. Then, as pointed out above, when 1 bit of error takes place in the read data, the error is corrected, and the read data is sent as internal output data do0-do31 to data output buffer DOB (to be explained later). When 2 bits of error take place, the errors are detected but not corrected. When the error is detected in the read data, the ECC circuit sends the high-level internal error detection signal ed to timing generation circuit TG. Although there is no particular limitation in this respect, when internal error detection signal ed is set to the high level, timing generation circuit TG sends the low-level error detection signal $\overline{ED}$ to a memory control unit (not shown in the figure).

Internal output data do0-do31 is sent from said ECC circuit to data output buffer DOB, and timing signal ϕoe is sent from timing generation circuit TG.

Since said timing signal ϕoe is set to the high level, the data output buffer DOB is selectively set to the operating state. In this operating state, data output buffer DOB forms the output signal according to said internal output data do0-do31, and sends the signal from data input/output terminals D0-D31 to a memory control unit (not shown in the figure). Although there is no

particular limitation in this respect, when timing signal ϕoe is set to the low level, the output of data output buffer DOB is set to the high-impedance state.

On the basis of chip enable signal $\overline{CE}$ and write enable signal $\overline{WE}$ sent from a memory control unit (not shown in the figure), timing generation circuit TG forms the aforementioned various timing signals and internal control signals, which are then sent to the various circuits. As pointed out above, when high-level internal error detection signal ed is sent from the ECC circuit, low-level error detection signal ED is sent to the memory control unit.

Figure 2 is a block diagram illustrating an application example of the ECC circuit (ECC) of Figure 1.

There is no particular limitation on the ECC circuit of this application example. However, it should contain data selection circuit SEL, check bit generation circuit CG, syndrome generating circuit SG, and data correcting circuit DC. In this application example, there is no particular limitation on the type of the exclusive-OR circuit for forming check bits cw0-cw6 in the write operation. However, in the read operation, check bit generation circuit CG is shared with the exclusive-OR circuit for receiving the prescribed bits of said internal read data dr0-dr31 as a portion of the error correcting circuit which checks the state of the read data in the read operation. Said syndrome generating circuit SG contains a circuit for forming syndromes s0-s6 on the basis of the output signal of the aforementioned exclusive-OR circuit, that is, a portion of the error correcting circuit, and internal read check bits cr0-cr6 fed from read amplifier RAS.

Data correction circuit DC contains the circuit for correcting the error in internal read data dr0-dr31 according to said syndromes s0-s6.

In Figure 2, there is no particular limitation on the type of data selection circuit SEL, which, however, should contain first and second selection gates made of 32 clocked inverter circuits each. For the 32 clocked inverter circuits forming the first selection gate, their input terminals receive corresponding internal input data di0-di31, respectively, from said data input buffer DIB. On the other hand, the input terminals of the 32 clocked inverter circuits that form the second selection gate receive corresponding internal read data dr0-dr31 from said read amplifier RAD. The output terminals of the 32 clocked inverter circuits that form the first selection gate are commonly coupled to the output terminals of the 32 corresponding clocked inverter circuits that form the second selection gate. According to internal control signal wm fed from timing generation circuit TG, the 32 clocked inverter circuits that form the first selection circuits are selectively set to the transmitting state. On the other hand, according to the inverted signal of the aforementioned internal control signal wm, the 32 clocked inverter circuits that form the second selection circuits are selectively set to the transmission state.

Consequently, for data selection circuit SEL, when memory unit MU is set to the write operation mode, and said internal control signal wm is set to the high level, internal input data di0-di31 fed from data input buffer DIB are selected, and they are sent as internal data dc0-dc31 to check bit generation circuit CG. When memory unit MU is set to the read operation

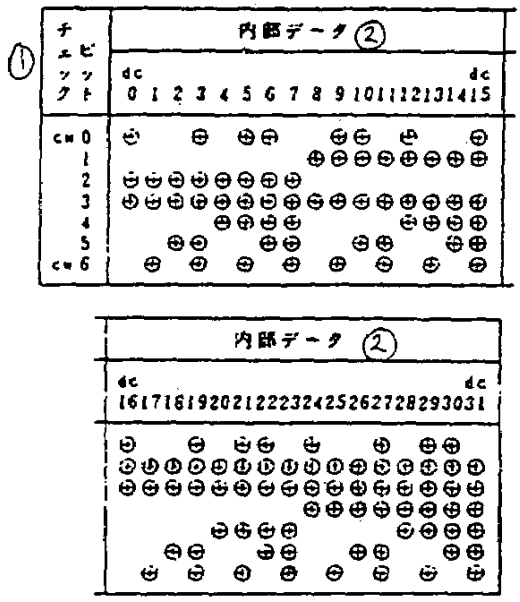
mode, and said internal control signal wm is set to the low level, internal read data dr0-dr32 fed from read amplifier RAD is selected and sent as internal data dc0-dc31 to check bit generation circuit CG.

Check bit generation circuit CG contains 7 exclusive-OR circuits for receiving with a prescribed combination the internal data dc0-dc31 fed from said data selection circuit SEL. The output signals of the exclusive-OR circuits are taken as said check bits cw0-cw6. In the ECC method of this invention, as pointed out above, the single-error correction/double-error detection method is adopted, and check bit cw0-cw6 are formed according to the algorithm listed in Table I.

That is, as shown in Table I, check bits cw0 is formed as the result of the exclusive-OR operation for the 16 internal data dc0, dc3, dc5 ..., dc30 annexed with mark ⊕ among the internal data dc0-dc31. Check bit cw1 is formed as the result of the exclusive-OR operation for the 24 internal data dc8-dc31 annexed with mark ⊕. Similarly, other check bits cw2-cw6 are formed as the result of the exclusive-OR operation for the prescribed number of internal data annexed with mark ⊕.

When the memory unit MU is set to the write operation mode, check bits cw0-cw6 output from check bit generation circuit CG are fed to said write amplifier WAS and are written into the assigned address in check bit memory CM. In this case, said internal input data di0-di31 are written at the same time into the corresponding addresses of data memory DM. On the other hand, when memory unit MU is set to the read operation mode, check bits cw0-cw6 are fed to syndrome generating circuit SG of the ECC circuit, and are used in forming syndromes s0-s6.

Table I



Key: 1. Check bit
2. Internal data

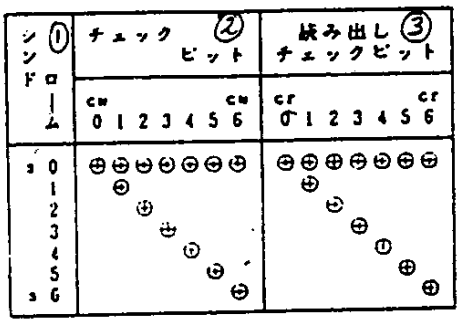
Check bits cw0-cw6 generated by said check bit generation circuit CG are fed to syndrome generating circuit SG, and internal read check bits cr0-cr6 are fed from read amplifier RAS of said check bit memory CM.

When memory unit MU is set to the read operation mode, syndrome generating circuit SG is set selectively to the operating state. In this operating state, syndrome generation circuit SG generates syndromes s0-s6 on the basis of said check bits cw0-cw6 and internal read check bits cr0-cr6. There is no particular limitation on these syndromes s0-s6. However, they

should be respectively generated according to the algorithm listed in Table II.

That is, as listed in Table II, syndrome s0 is formed as the result of the exclusive-OR operation of all of check bits cw0-cw6 and internal read check bits cr0-cr6. Syndrome s1 is formed as the result of the exclusive-OR operation for check bit cw1 and internal read check bit cr1. Similarly, other syndromes s2-s6 are formed as the result of the exclusive-OR operation for check bits cw2-cw6 and the corresponding internal read check bits cr2-cr6, respectively.

Table II



Key: 1. Syndrome
2. Check bit
3. Read check bit

Said syndromes s0-s6 formed by syndrome generation circuit SG are fed to data correcting circuit DC.

While said syndromes s0-s6 are fed from said syndrome generation circuit SG to data correcting circuit DC, internal

read data dr0-dr31 is also sent from read amplifier RAD of said data memory DM.

When memory unit MU is set to the read operation mode, data correcting circuit DC is set selectively to the operating state. In this operating state, based on said syndromes s0-s6, data correcting circuit DC determines the state of internal read data dr0-dr31 and internal read check bits cr0-cr6. According to the result, the error of internal read data dr0-dr31 is corrected, and the data is then sent as internal output data do0-do31 to data output buffer DOB.

That is, when syndrome s0 is at logic "0" and all the other syndromes s1-s6 are at logic "0," [data correcting circuit DC] determines that there are no errors in internal read data dr0-dr31 and internal check bits cr0-cr6. On the other hand, when syndrome s0 is at logic "0" while any one of the other syndromes s1-s6 is at logic "1," data correction circuit [DC] determines that there are two errors, that is, a double error, in internal read data dr0-dr31 and internal check bits cr0-cr6. In addition, when syndrome s0 is at logic "1" while several of the other syndromes s1-s6 are at logic "1," data correction circuit DC determines that there is a single error in internal read data dr0-dr31. In this case, according to the algorithm listed in Table III, data correction circuit DC specifies the error bit in internal read data dr0-dr31.

For example, when syndrome s0 is at logic "1," and syndromes s2 and s3 are at logic "1" at the same time, data correcting circuit DC determines that an error has taken place in internal read data dr0. Consequently, said internal read data dr0 fed from read amplifier RAS is inverted to internal output data do0.

Similarly, when, e.g., syndrome s0 is at logic "1" and all of the other syndromes s1-s6 are also at logic "1", data correcting circuit DC determines that an error takes place in internal read data dr31. Consequently, internal read data dr31 fed from read amplifier RAS is inverted to internal output data do31.

When syndrome s0 is at logic "1" while all of the other syndromes s1-s6 are at logic "0," data correction circuit DC determines that an error has taken place in read check bit cr0. When syndrome s0 is at logic "1" while only one of the other syndromes s1-s6 is at logic "1," data correction circuit DC determines that an error has taken place in [one of the] read check bits cr1-cr6 corresponding to a syndrome from syndromes s1-s6 at logic "1."

Table III

s 0 = 1

s 6	s 5	s 4					
			s 1	0	1	1	1
			s 2	1	0	1	1
			s 3	1	1	0	1
0	0	0	-	dr 0	dr 8	dr16	dr24
1	0	0	-	dr 1	dr 9	dr17	dr25
0	1	0	-	dr 2	dr10	dr18	dr26
1	1	0	-	dr 3	dr11	dr19	dr27
0	0	1	-	dr 4	dr12	dr20	dr28
1	0	1	-	dr 5	dr13	dr21	dr29
0	1	1	-	dr 6	dr14	dr22	dr30
1	1	1	-	dr 7	dr15	dr23	dr31

Figure 3 illustrates the timing in an application example of the write mode of the memory unit MU of Figure 1. In the following, we will present a brief explanation of the write operation mode of memory unit MU with reference to this figure.

As shown in Figure 3, when chip enable signal $\overline{CE}$ is changed from the high level to the low level, memory unit MU is set to the selected state. Before change of said chip enable signal $\overline{CE}$, the write enable signal $\overline{WE}$ is set to the low level. Also, with low address "r" and column address "c" in an assigned combination, X-address signals AX0-AXi and Y-address signals AY0-AYj are sent to external terminals AX0-AXi and AY0-AYi, and write data wd is sent to data input/output terminals D0-D31.

In memory unit MU, since chip enable signal $\overline{CE}$ is set to the low level, timing signals ϕxd, ϕxs, and ϕys and internal control signal wm are set to the high level. Also, after said timing signals ϕxd, ϕpa and ϕyd are set to the high level with a short delay. After said timing signal ϕyd is sent with a short delay, timing signal ϕwd is temporarily set to the high level. In addition, at the time when the operation of the formation of the internal write check bits cw0-cw6 is ended by executing of ECC circuit, timing signal ϕws is temporarily set to the high level.

Since timing signal ϕxd is set to the high level, the word line selection operation of memory array MARYD is started in data memory DM of memory unit MU. In this way, word line Wr set at row address "r" of memory array MARYD is alternately set to the high-level selected state. According to the memory data, the low amplitude read signals are read from the 32 x (n + 1) memory cells coupled to said word line Wr on the various complementary data lines of memory array MARYD. Since timing signal ϕpa is set

to the high level, these low amplitude read signals are amplified by the corresponding unit amplifiers of sense amplifier SA to form high-level or low-level binary read signals.

Then, since timing signal ϕyd is set to the high level, data selecting signals YD0-YDn are alternately set to the high level, and the 32 groups of complementary data lines corresponding to column address "c" of memory array MARYD are connected to the corresponding unit circuits of write amplifier WAD through the corresponding complementary common data lines CDD0-CDD31. In this way, the 32 memory cells set at address "rc" of memory array MARYD are respectively set to the selected state and connected to the corresponding unit circuits of write amplifier WAD. Since timing signal ϕwd is set temporarily to the high level, internal input data di0-di31 are written respectively into these memory cells. This write operation is carried out with a relatively long access time of data memory DM and with a notification the check bit generation operation by the ECC circuit.

On the other hand, when timing signals ϕxs and ϕys are set to the high level, in check bit memory CM of memory unit MU, the address selection operation of memory array MARYS is started by means of X-address decoder XADS and Y-address decoder YADS. In addition, at the same time, the operation for generating the check bits is executed by the ECC circuit. In this case, as pointed out above, as internal control circuit wm is set to the high level, internal input data di0-di31 are input to the ECC circuit. The check bits formed by the ECC circuit are sent as internal write check bits cw0-cw6 to write amplifier WAS of check bit memory CM.

However, since the number of logic stages in the exclusive-OR circuit set in check bit generation circuit CG is large, a relatively long time is needed to perform the operation of generating the check bits by the ECC circuit. Consequently, address selection by check bit memory CM is carried out parallel to the check bit generation by the ECC circuit. However, as pointed out above, memory array MARYS of check bit memory CM is composed of static memory cells which allow relatively high operation speeds. Consequently, address selection by check bit memory CM ends virtually faster than the check bit generation, by the ECC circuit.

At the point in time when the address selection operation of check bit memory CM ends and the check bit generation operation by the ECC circuit ends, since timing signal ϕws is temporarily set to the high level, write amplifier WAS of check bit memory CM is set to the operating state. Consequently, with respect to the 7 memory cells in address "rc" of check bit memory CM, the write operation of internal write check bits cw0-cw6 fed from check bit generating circuit CG is executed.

In this case, the access time of data memory DM is almost equal to the sum of the time needed for the check bit generation operation by means of the ECC circuit and the access time of check bit memory CM. Consequently, although memory array MARYD of data memory DM is composed of dynamic memory cells with a relatively slow operating time and the check bits are formed by the check bit generating circuit with a relatively long operating time as compared to the write data, the requirement for the overall access time of memory unit MU can be met by the data memory DM by itself.

As explained above, memory unit MU in this application example contains the ECC circuit. The write data fed via the memory control unit is composed of 32 bits, and 7 ECC check bits are annexed to this write data. In this application example, the aforementioned write data is written into data memory DM composed of dynamic memory cells with relatively long access time, and the check bits are written into check bit memory CM made of static memory cells with a relatively short access time. Consequently, although check bit generation is performed via a check bit generation circuit with a relatively long operational time in series with the address operation of check bit memory CM, the access time of memory unit MU in the write operation depends only on the access time of data memory DM. As a result, the speed of operation can be increased for the access time of memory unit MU containing the ECC circuit, and the cycle time of digital processing equipment containing memory unit MU can be cut.

As indicated in the aforementioned application example, when this invention is applied to a semiconductor memory device, such as a RAM, used as the memory unit of digital processing equipment containing an ECC circuit, the following effects can be achieved.

(1) In RAM or other semiconductor memory device containing an ECC circuit, a memory array for containing the input data and a memory array for containing the check bits formed corresponding to the aforementioned input data are arranged separately. The aforementioned memory array for containing the check bits is composed of memory cells which allow higher speeds of operation than the memory array for containing the input data. Consequently, the sum of the access time of the memory array for containing the check bits and the operating time needed for

generating the check bits of the ECC circuit is almost equal to the access time of the memory array for containing the input data.

(2) Due to said effect (1), the access time for the write operation of RAM or other semiconductor memory device containing an ECC circuit can be significantly reduced.

(3) Due to said effects (1) and (2), it is possible to shorten the cycle time of digital processing equipment containing the memory unit made of RAM or other semiconductor memory devices containing an ECC circuit, and to improve its processibility.

In the above, this invention has been explained in detail with reference to an application example. However, this invention is not limited to said application example. Variations are possible as long as the main concept of this invention is observed. For example, as shown in the block diagram of Figure 1, data memory DM and check bit memory CM may also be made of MOS static memory cells and bipolar memory cells, respectively. Various types of memory cells may be combined as long as the sum of the access time of check bit memory CM and the operating time of the ECC circuit is equal to the operating time of data memory DM. Also, the address decoders in data memory DM and check bit memory CM may be partially shared. Memory arrays MARYD and MARYS may be composed of multiple memory mats, respectively. Memory unit MU may be formed on multiple semiconductor substrates instead of a single semiconductor substrate. As shown in the block diagram of Figure 2, the exclusive-OR circuit for generating the check bits may also be arranged in both check bit generation circuit CG and syndrome generating circuit SG. In this case, there is no need for data selection circuit SEL. As

far as the ECC method is concerned, a single-error correction method, which is unable to detect double errors, may be used. In addition, various forms of implementation may be adopted for the combination of the various control signals and address signals, as well as the block configuration of memory unit MU shown in Figure 1 and the block configuration of the EEC circuit shown in Figure 2.

In the above, an explanation was given mainly for the case in which a RAM or another semiconductor memory device was used for the memory units in digital processing equipment as the background application field of this invention. However, the application is not limited to this case. For example, the semiconductor memory device of this invention may also be used for a buffer memory used in laser printers and other digital equipment. That is, this invention can be widely applied in manufacturing the semiconductor memory devices containing at least an ECC circuit and digital equipment containing the aforementioned semiconductor memory devices.

Effects of the invention

The effects of this invention as disclosed above can be simply summarized. That is, in the RAM or another semiconductor memory device containing an ECC circuit, the memory array containing the input data and the memory array containing the check bits generated corresponding to the aforementioned input data are arranged separately. The aforementioned memory array containing check bits is made of memory cells that allow higher speed of operation than the aforementioned memory array

containing the input data. With this configuration, the access time of the write operation of RAM or another semiconductor memory device containing an ECC circuit can be significantly shortened, the cycle time of digital equipment containing this type of RAM or other semiconductor memory device can be cut, and its processibility can be improved.

Brief explanation of the figures

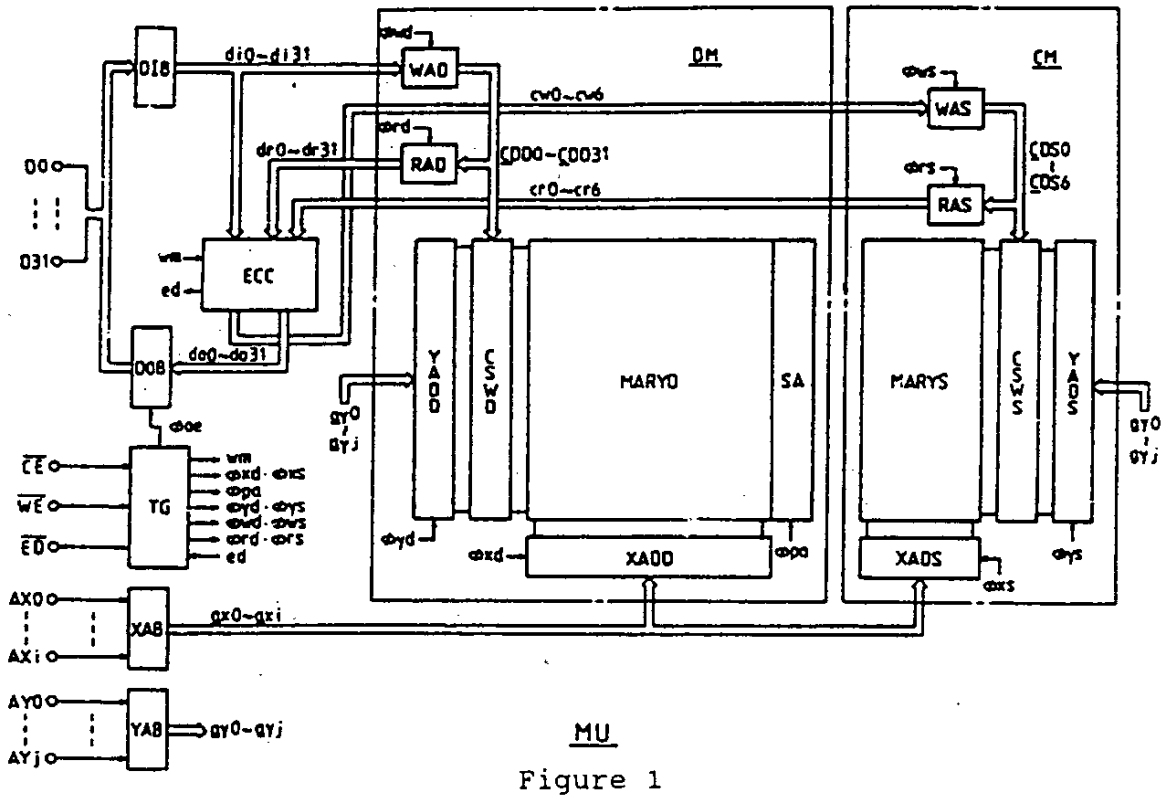
Figure 1 is a block diagram illustrating an application example of the memory unit composed of RAM of this invention.

Figure 2 is a block diagram of an application example of the ECC circuit in the memory unit shown in frequency 1.

Figure 3 is a timing chart illustrating an application example of the write operation of the memory unit shown in Figure 1.

MU, memory unit
DM, data memory
CM, check bit memory
MARYD, MARYS, memory arrays
SA, sense amplifier
CSWD, CSWS, column switches
XADD, XADS, X-address decoders
XAB, X-address buffer
YADD, YADS, Y-address decoders
YAB, Y-address buffer
WAD, WAS, write amplifiers
RAD, RAS, read amplifiers

DIB, data input buffer
DOB, data output buffer
TG, timing generation circuit
ECC, ECC circuit
SEL, data selection circuit
CG, check bit generation circuit
SG, syndrome generation circuit
DC, data correction circuit



MU

Figure 1

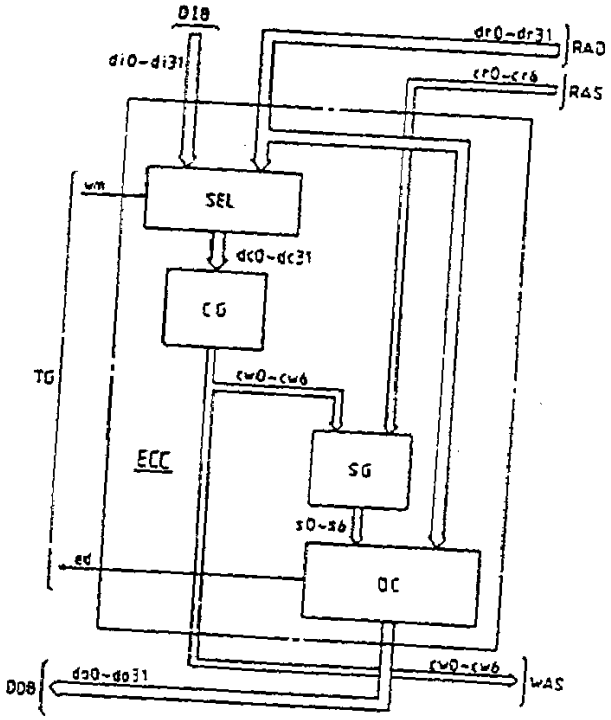

DI8
di0~di31
dr0~dr31
RA0
cr0~cr6
RAS
wn
SEL
dc0~dc31
CG
TG
cw0~cw6
ECC
SG
s0~s6
ed
DC
DO8
do0~do31
cw0~cw6
WAS

Figure 2

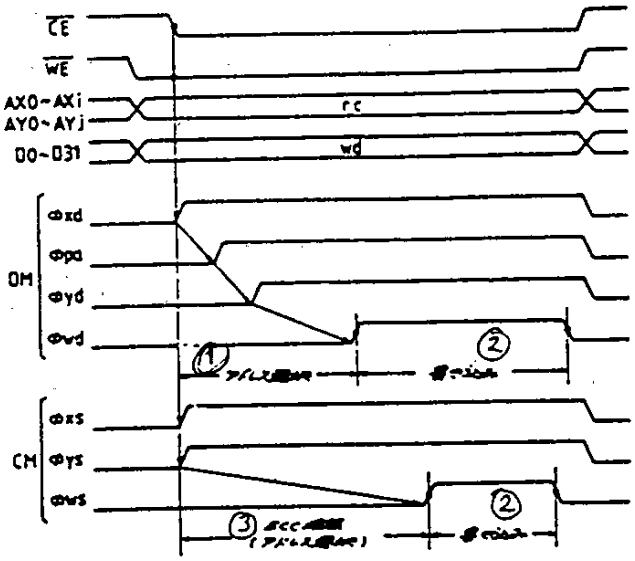


Figure 3

Key: 1. Address selection
2. Write
2. ECC [illegible] (address selection)